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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,306	11/04/2003	Hea Suk Jung	CU-3424 VE	5038

26530 7590 05/12/2005

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EXAMINER
NGUYEN, LINH M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/701,306	JUNG, HEA SUK	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2005 and 16 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-13 are pending in the instant application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 7-8, 10, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. , "A Low-Noise CMOS Prescaler for 900 MHz to 1.9 GHz Wireless Applications", IEEE 1999 Custom Integrated Circuits Conference, pp. 597-600.

With respect to claim 1, Chang et al. discloses, in Fig. 1, clock divider for a DLL (Delay Lock Loop) circuit of a synchronous memory device for synchronization an external input clock with an internal input clock, wherein the synchronous memory device generates a control signal indicative of the power down condition of the synchronous memory device, the clock divider comprising a) M number of dividers [x8, x9, x10, x11] connected in series; the serially connected dividers being consecutively referred to as first to Mth dividers, wherein a first clock signal is inputted to the first divider and the first divider outputs to the second divider a clock signal having half the first clock signal frequency, and wherein each of the second to M-th divider receives the clock signal outputted from the formerly connected divider and outputs to the subsequently connected divider a clock signal frequency, and b) power-down controller [X12] for receiving the control signal [s], an output signal of the (M-1)-th divider [x10] and an output signal of the M-th divider [x11], and selectively outputting an output signal.

With respect to claim 2, Chang et al. discloses, in Fig. 1, that the output signal of the power-down controller has frequency obtained by dividing the frequency of the first clock signal divider into $1/2^{M}$ or $1/2^{(M-1)}$ in accordance with a logic level of the control signal.

With respect to claim 3, Chang et al. discloses, in Fig. 1, that when the logic level the control signal [s] is inn a first state (high level), the output signal the power-down controller becomes the output signal of the (M-1)-th divider, and when the logic level of the control signal is in a second state (low level), the output signal of the power-down controller becomes the output signal of the M-th divider.

With respect to claim 4, Chang et al. discloses, in Fig. 1, that the control signal is a clock enable signal used in the synchronous memory device.

With respect to claims 5, 8, 10 and 12, Chang et al. discloses, in Fig. 1, that a pulse width of a high-level state any one of claims output signal of the first divider [x8] is the same as a period of the input signal [clock input of x8] of the first divider, and a pulse width of a low-level state of output signals of the second [x9] to M-th [x11] dividers the same as the period of the input signal of the first divider *(via division by 2 process)*.

With respect to claim 7, Chang et al. discloses, in Fig. 1, a clock divider and a control signal indicative of the power down condition of the synchronous memory device, the clock divider comprising M number of dividers connected in series, the serially connected dividers being consecutively referred to as first to M-th dividers, wherein a first clock signal is inputted to the first divider and the first divider outputs to the second divider a clock signal having half the first clock signal frequency, and wherein each of the second to M-th divider receives the clock signal outputted from the formerly connected divider and outputs to the subsequently connected

divider a clock signal having the frequency that is half the inputted clock signal frequency, a clock dividing method comprising a steps of outputting an output signal of a (M-1)-th divider [x10] of the clock divider when the control signal is in the first state; and outputting an output signal of an M-th divider [X11] as the output signal of the clock divider when the control signal is in the second state.

With respect to claim 13, Chang et al. discloses, in Fig. 1, a clock buffer part [x6] receiving the external input clock, wherein the external input clock passed through the clock buffer part is the first clock.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Chang et al. ("A Low-Noise CMOS Prescaler for 900 MHz to 1.9 GHz Wireless Applications", IEEE 1999 Custom Integrated Circuits Conference, pp. 597-600) in view of Tran (U.S. Patent No. 5,162,666).

With respect to claims 6, 9 and 11, Chang et al. discloses all of the claimed limitations as expressly recited in claim 1 *(the examiner presumes that claim 6 is dependent on claim 1, see Claim Objection)* except for the power-down controller comprises two transmission gates, and the two transmission gates are selectively turned on/off according to the control signal.

Tran discloses, in Fig. 2, a power-down controller [80] comprises two transmission gates, and the two transmission gates are selectively turned on/off according to a control signal [S1].

To configure the circuit of Chang et al. with a power-down controller as taught by Tran for providing a multiplexing function would have been obvious to one of ordinary skill in the art at the time of the invention since Tran teaches that such configuration would minimize loading on select signal lines *(see Tran, col. 1, lines 57-58).*

Remarks

5. Applicant's arguments filed 03/16/2005 and 03/30/2005 have been fully considered but they are not persuasive.

With respect to the Applicant's argument regarding claims 1 and 7, at page 11, first paragraph, the Applicant stated that " *Nowhere in Chang teaches or suggests the claimed –control signal indicative of the power down mode- and further does not teach or suggest its "prescaler" behaving differently based on the status of the claimed –control signal–".* Chang discloses, in Fig. 1, the control signal [S] to control [X12], which is the equivalent component as this so-called "power down controller" [500] as indicated in the claimed invention. The control signal [s] and the flip-flop [x12] in Chang are not called "power-down control signal" and "power down controller", respectively; however, the subject matter need not be described or called literally in order for the disclosure to satisfy the claimed requirement as long as they are very much similar components with equivalent functions. Regarding the later part of the Applicant's argument "*Chang does not teach or suggest its "prescaler" behaving differently based on the status of the claimed –control signal–".* This limitation is not in the claims and should not be since the "dividers" (/presaler) do not (/does not) behave differently based on the

control signal, only the output of the "power-down controller" [500] of the claimed invention outputs differently depending on the control signal.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER